



05/28/99

Please type a plus sign (+) inside this box →



PTO/SB/05 (1/98)

Approved for use through 09/30/2000. OMB 0651-0032  
Patent and Trademark Office U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

<b>UTILITY PATENT APPLICATION TRANSMITTAL</b>  <i>(Only for new nonprovisional applications under 37 CFR 1.53(b))</i>		Attorney Docket No. <b>0756-1974</b>  First Inventor or Application Identifier: <b>Yasuhiko TAKEMURA et al.</b>  Title: <b>SEMICONDUCTOR DEVICE AND PROCESS FOR FABRICATING THE SAME</b>  Express Mail Label No.	
<b>APPLICATION ELEMENTS</b> See MPEP chapter 600 concerning utility patent application contents.		<b>ADDRESS TO:</b> Assistant Commissioner for Patents Box Patent Application Washington, DC 20231	
1. <input checked="" type="checkbox"/> Fee Transmittal Form (e.g., PTO/SB/17) <i>(Submit an original, and a duplicate for fee processing)</i> 2. <input checked="" type="checkbox"/> Specification <span style="float: right;">Total Pages [44]</span> <i>(preferred arrangement set forth below)</i> - Descriptive title of the Invention - Cross References to Related Applications - Statement Regarding Fed sponsored R & D - Reference to Microfiche Appendix - Background of the Invention - Brief Summary of the Invention - Brief Description of the Drawings (if filed) - Detailed Description - Claim(s) - Abstract of the Disclosure 3. <input checked="" type="checkbox"/> Drawing(s) (35 USC 113) <span style="float: right;">Total Sheets [6]</span> 4. <input checked="" type="checkbox"/> Oath or Declaration <span style="float: right;">Total Pages [2]</span> a. <input type="checkbox"/> Newly executed (original or copy) b. <input checked="" type="checkbox"/> Copy from a prior application (37 CFR 1.63(d)) <i>(for continuation/divisional with Box 17 completed)</i> [Note Box 5 below] i <input type="checkbox"/> <b>DELETION OF INVENTOR(S)</b> Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b). 5. <input checked="" type="checkbox"/> Incorporation By Reference (useable if Box 4b is checked) The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered to be part of the disclosure of the accompanying application and is hereby incorporated by reference therein.		6. <input type="checkbox"/> Microfiche Computer Program (Appendix)  7. Nucleotide and/or Amino Acid Sequence Submission <i>(if applicable, all necessary)</i> a. <input type="checkbox"/> Computer Readable Copy b. <input type="checkbox"/> Paper Copy (identical to computer copy) c. <input type="checkbox"/> Statement verifying identity of above copies  <hr/> <b>ACCOMPANYING APPLICATION PARTS</b>  8. <input type="checkbox"/> Assignment Papers (cover sheet & document(s)) 9. <input type="checkbox"/> 37 CFR 3.73(b) Statement <span style="float: right;"><input type="checkbox"/> Power of Attorney</span> <i>(when there is an assignee)</i> 10. <input type="checkbox"/> English Translation Document (if applicable) 11. <input checked="" type="checkbox"/> Information Disclosure Statement <span style="float: right;"><input type="checkbox"/> Copies of IDS</span> (IDS)/PTO-1449 <span style="float: right;">Citations</span> 12. <input checked="" type="checkbox"/> Preliminary Amendment 13. <input checked="" type="checkbox"/> Return Receipt Postcard (MPEP 503) <i>(Should be specifically itemized)</i> 14. <input type="checkbox"/> *Small Entity <span style="float: right;"><input type="checkbox"/> Statement filed in prior application,</span> Statement(s) <span style="float: right;">Status still proper and desired</span> (PTO/SB/09-12) 15. <input type="checkbox"/> Certified Copy of Priority Document(s) <i>(if foreign priority is claimed)</i> 16. <input checked="" type="checkbox"/> Other: Notice of Change of Address  *A new statement is required to be entitled to pay small entity fees, except where one has been filed in a prior application and is being relied upon.	
17. If a <b>CONTINUING APPLICATION</b> , check appropriate box, and supply the requisite information below and in a preliminary amendment Divisional of prior application Serial No. 08/853,187, filed April 29, 1997; which itself is a Divisional of Serial No. 08/671,499, filed June 27, 1996, now U.S. Patent No. 5,661,311; which itself is a Divisional of Serial No. 08/287,259, filed August 8, 1994, now U.S. Patent No. 5,569,935. Prior application information: Examiner: <u>M. Wilczewski</u> <span style="float: right;">Group/Art Unit: <u>2822</u></span>			
<b>18. CORRESPONDENCE ADDRESS</b>			
<div style="display: flex; justify-content: space-between;"> <span><input checked="" type="checkbox"/> Customer Number or Bar Code Label</span> <span>Customer No. 22204</span> <span>or <input type="checkbox"/> Correspondence address below</span> </div> <div style="text-align: center; margin-top: 5px;"> <i>(Insert Customer No. or Attach bar code label here)</i> </div>			
Name: Eric J. Robinson Firm: SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, P C Address: 8180 Greensboro Drive, Suite 800 City: McLean State VA Zip Code 22102 Country: U S A Telephone (703) 790-9110 FAX (703) 883-0370			
Name: Eric J. Robinson		Registration No. 38,285	
Signature		Date: May 27, 1999	

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

jc525 U.S. PTO  
09/321715

05/28/99

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re DIVISIONAL Application of )  
Yasuhiko TAKEMURA et al. )  
Based On Serial No. 08/853,187 ) Art Unit: 2822  
Which Was Filed: April 29, 1997 ) Examiner: M. Wilczewski  
For: SEMICONDUCTOR DEVICE AND )  
PROCESS FOR FABRICATING )  
THE SAME ) Date: May 27, 1999

PRELIMINARY AMENDMENT

Honorable Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

Please preliminarily amend the subject application as follows:

IN THE SPECIFICATION:

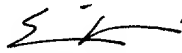
Before the first sentence of the specification, insert --This application is a Divisional application of Serial No. 08/853,187, filed April 29, 1997; which itself is a Divisional of Serial No. 08/671,499, filed June 27, 1996, now U.S. Patent No. 5,661,311; which itself is a Divisional of Serial No. 08/287,259, filed August 8, 1994, now U.S. Patent No. 5,569,935.--

REMARKS

This application has been amended to include the continuing application data thereof.

Examination on the merits is requested.

Respectfully submitted,



---

Eric J. Robinson  
Registration No. 38,285

Sixbey, Friedman, Leedom & Ferguson, P.C.  
8180 Greensboro Drive, Suite 800  
McLean, Virginia 22102  
(703) 790-9110

662220 0756-1974

## TITLE OF THE INVENTION

SEMICONDUCTOR DEVICE AND PROCESS FOR FABRICATING THE  
SAME

## BACKGROUND OF THE INVENTION

### 1. Field of the Invention

The present invention relates to a structure of a semiconductor integrated circuit comprising at least two thin film transistors (abbreviated hereinafter as "TFTs") on a same substrate, and to a process for fabricating the same. The semiconductor integrated circuit according to the present invention is utilized, for example, in active matrices of liquid crystal displays.

### 2. Prior Art

Prior art TFTs have been fabricated heretofore by patterning a thin film semiconductor region (active layer) into an island-like shape to isolate the region from other TFTs, depositing an insulating film as a gate dielectric on the region by CVD or

sputtering, and then forming thereon a gate electrode.

Fig. 2 shows the process for fabricating a semiconductor integrated circuit comprising a TFT according to a prior art process. Referring to Fig. 2, a base film 22 and a silicon film 23 are formed on a substrate 21. Then, films 24a and 24b made of a material such as a photoresist are formed selectively on the silicon film 23. A thin film of silicon oxide or silicon nitride can be formed between the silicon film 23 and the films 24a and 24b to prevent the silicon film from being polluted (Fig. 2 (A)).

The silicon film 23 is etched thereafter to form island-like silicon regions (active layers) 25a and 25b using the films 24a and 24b as the masks, however, the base layer 22 is etched partially at the same time. Thus, the step height increases by the over-etched portion x in addition to the thickness of the silicon film (Fig. 2 (B)).

Then, an insulating film 26 which functions as a gate dielectric is formed over the entire surface to form a gate electrode with lines 27n, 27p, and 27c. Line disconnection may occur in case the active layer is provided with too large a step

height.

After forming the gate electrode, impurities are introduced by means of, for example, ion doping or ion implantation. The resulting structure thus obtained is subjected to activation treatment by, for example, thermal annealing, laser annealing, or lamp annealing to form impurity regions 28n (n-type) and 28p (p-type).

Subsequently, an interlayer insulator 29 is deposited to form contact holes therethrough, and electrodes 30a, 30b, and 30c are formed in the impurity regions of the TFT.

In the prior art processes, however, the overetching of the base film has been found a problem. The presence of a step due to the overetching causes disconnection on the gate electrode to considerably impair the product yield. A step with a further increased step height produces in particular when a film having a high etching rate is used as the base film. Accordingly, though the use of a film deposited by plasma CVD or APCVD is preferred as the base film from the mass productivity point of view, these types of films are not preferred from the aforementioned problem of high

etching rate. Thus, an object of the present invention is to review the problems in the prior art process for element isolation, and to provide a TFT of high product yield and a process for fabricating the same.

#### SUMMARY OF THE INVENTION

The present invention comprises electrically isolating the elements (e.g. the transistors) from each other not by cutting the silicon film but by selectively and thermally oxidizing the silicon film in the temperature range of from 500 to 650 °C. The silicon film to be oxidized may be either an amorphous film or a crystalline film. The silicon film is provided at a thickness of from 100 to 1,500 Å, and more preferably, at a thickness of 500 Å or less. A glass substrate having a thermal deformation point (strain point) of 750 °C or lower, which is represented by a Corning 7059 glass (an alkali-free borosilicate glass), is used as the substrate.

What is to be noted here is that a non-single crystal silicon, for example, an amorphous or a polycrystalline silicon, yields a

thermal oxidation rate which is about twice as large as that of a single crystal silicon. In the present invention, furthermore, from 0.1 to 100 % of water is added into the atmosphere to increase the oxidation rate. The addition of water increases the oxidation rate by about 10 times as compared with that in a dry atmosphere. Fig. 5 shows the relation between the thickness of silicon oxide obtained by the oxidation process (under a water vapor partial pressure of 100 %) according to the present invention and the duration of process. The figure reads that the silicon film according to the present invention can be entirely oxidized at a temperature as low as in the range of from 550 to 600 °C.

The oxidation reaction can be furthermore accelerated by effecting the oxidation while applying a pressure in the range of from 1 to 15 atm. For instance, an oxidation rate 10 times the rate of oxidation under a pressure of 1 atm can be obtained under a pressure as high as 10 atm. The temperature of oxidation can be also lowered. The change in oxidation rate under a pressure of 4 atm is also shown in Fig. 5. The quantity of water vapor can be



stabilized by performing the so-called pyrogenic oxidation process. This process comprises generating water vapor by the combustion of pure hydrogen. The concentration of water vapor in the atmosphere can be determined by controlling the flow rate of hydrogen.

The silicon film can be selectively oxidized by selectively forming on the silicon film a mask film comprising a silicon nitride layer or multilayered structure comprising a silicon oxide layer and a silicon nitride layer provided on the silicon oxide layer, and exposing the silicon film to a thermally oxidizing atmosphere using the mask film. No oxidation reaction proceeds on the surface thus covered with the mask.

Thus, as mentioned in the foregoing, the process according to the present invention comprises forming the oxide by thermal oxidation. Accordingly, no steps as those generated during the etching of conventional silicon films are found to form during the process according to the present invention. Thus, disconnection of gate electrodes is prevented from occurring, and the yield is

therefore increased. In particular, the process according to the present invention is almost free from the influence of the base film. Accordingly, the total mass production can be improved without being limited by the film deposition process.

#### BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1 (A) to 1 (E) show the step-sequential schematically drawn views for the structures obtained during fabrication of a TFT according to Example 1 of the process of the present invention;

Figs. 2 (A) to 2 (D) show the step-sequential schematically drawn views of the structures obtained during fabrication of a TFT according to a prior art process;

Figs. 3 (A) to 3 (E) show the step-sequential schematically drawn views for the structures obtained during fabrication of a TFT according to Example 2 of the process of the present invention;

Figs. 4 (A) to 4 (E) show the step-sequential schematically drawn views for the structures obtained during fabrication of a TFT according to Example 3 of the process of the present invention;

Fig. 5 is a graph showing the progress of thermal oxidation on a polycrystalline silicon film at a low temperature of 600 °C or lower under the presence of water vapor; and

Figs. 6 (A) to 6 (E) show the step-sequential schematically drawn views for the structures obtained during fabrication of a TFT according to Example 4 of the process of the present invention.

#### EXAMPLE 1

Referring to Figs. 1 (A) to 1 (E), the process according to the present Example is described below. Figs. 1 (A) to 1 (D) show the cross section structures, and Fig. 1 (E) shows the top view.

A Corning 7059 glass substrate 10 was heated to a temperature range higher than the deformation point thereof. Thus, the substrate was annealed in the temperature range of from 600 to 660 °C, e.g., at 640 °C, for a duration of from 1 to 4 hours, e.g., for 1 hour, and was gradually cooled at a rate of from 0.1 to 0.5 °C/min, for example, at a rate of 0.2 °C/min. The substrate was taken out from the heating chamber in the temperature range of

from 450 to 590 °C, more specifically, at 550 °C. The substrate is preferably taken out at a temperature not higher than the maximum temperature of the subsequent heat treatment steps. This heat treatment suppresses irreversible shrinking from occurring on the substrate in the later heat treatment steps.

The substrate 10 thus subjected to the treatment above was cleaned, and a 2,000 Å thick silicon oxide film was deposited as a base film 11 by means of sputtering. An intrinsic (I-type) amorphous silicon film (intrinsic non-single crystal silicon film) 12 was deposited on the substrate at a thickness of from 300 to 1,000 Å, for example, at a thickness of 500 Å, by effecting plasma CVD. A silicon nitride film from 500 to 2,000 Å in thickness, for instance at a thickness of 1,000 Å, was deposited continuously. The silicon nitride film thus obtained only was selectively etched to form mask films 13a and 13b (Fig. 1 (A)).

The silicon film was then annealed at 600 °C for a duration of 48 hours under a nitrogen gas atmosphere of 1 atm to crystallize the silicon film. The crystallized silicon film was then allowed to

stand in an oxygen atmosphere (oxidizing atmosphere) containing 10 % water vapor under a pressure of 1 atm while maintaining the temperature in the range of from 550 to 650 °C, representatively, at 600 °C, for a duration of from 3 to 5 hours. Thus, the region of the silicon film not covered by the mask film was completely oxidized to the bottom to form silicon oxide regions 14a to 14c. The pressure of the water vapor was controlled by pyrogenic oxidation. As a result, the silicon film was separated into regions 15a and 15b (Fig. 1 (B)).

The masks 13a and 13b were removed thereafter, and a 1,200 Å thick silicon oxide insulating film 16 was deposited on the silicon film by plasma CVD to provide a gate dielectric (gate insulating film) using tetraethoxysilane ( $\text{Si}(\text{OC}_2\text{H}_5)_4$ ; TEOS) and oxygen as the starting materials. Subsequently, a silicon film containing from 0.01 to 0.2 % phosphorus was deposited by means of LPCVD at a thickness of from about 3,000 to 8,000 Å, for example, at a thickness of 6,000 Å. The silicon film was patterned to form gate electrodes 17n, 17p, and 17c on the gate insulating

film.

Impurities for imparting the region either P- or N-conductive were introduced in a self-aligned manner by means of ion doping process (plasma doping process) into the isolated silicon regions constituting the source/drain and the channel using the gate electrodes as the mask. Phosphine ( $\text{PH}_3$ ) and diborane ( $\text{B}_2\text{H}_6$ ) were used as the doping gas. The dose was from  $1 \times 10^{15}$  to  $8 \times 10^{15}$   $\text{cm}^{-2}$ . Thus, in case phosphine was used, phosphorus was introduced at a dose of, more specifically,  $2 \times 10^{15}$   $\text{cm}^{-2}$ , while applying an accelerating voltage of from 60 to 90 kV, for example, a voltage of 80 kV. In case diborane was used, boron was introduced at a dose of  $5 \times 10^{15}$   $\text{cm}^{-2}$  while applying an accelerating voltage of from 40 to 80 kV, for instance, a voltage of 65 kV. The regions were each selectively doped with the element by covering the other region with a photoresist. Thus were obtained an N-type impurity region 18n and a P-type impurity region 18p to form a region for a P-channel TFT (PTFT) and region for an N-channel TFT (NTFT). The outer periphery of the active layer of each of the PTFT and the NTFT

is oxidized to the bottom as described above.

The region was then annealed by irradiating a laser beam. A KrF excimer laser operating at a wavelength of 248 nm and at a pulse width of 20 nsec was used in the present invention. However, the type of the laser is not only limited thereto, and any other type of laser can be used as well. The laser beam was irradiated from 2 to 10 shots per site, for example, 2 shots per site, at an energy density of from 200 to 400 mJ/cm<sup>2</sup>, for instance, at 250 mJ/cm<sup>2</sup>. The effect of laser annealing can be further enhanced by heating the substrate in the temperature range of from about 200 to 450 °C (Fig. 1 (C)).

A 6,000 Å thick silicon oxide film 19 was deposited by plasma CVD process thereafter as an interlayer dielectric. The interlayer dielectric may be made from a polyimide film or a double-layered film of silicon oxide and polyimide. Contact holes were formed thereafter to establish electrodes with wiring 20a, 20b, and 20c for the TFT using a metallic material, for example, a multilayered film of titanium nitride and aluminum. A semiconductor circuit

comprising the TFTs in a complementary arrangement was obtained by finally annealing the structure at a temperature of 350 °C for a duration of 30 minutes under a hydrogen gas atmosphere at a pressure of 1 atm (Fig. 1 (D)).

The plan view of the structure shown with a cross section structure in Fig. 1 (C) is given in Fig. 1 (E). The cross section structures seen along the dot-and-dash line in Fig. 1 (E) are given in Figs. 1 (A) to 1 (D).

## EXAMPLE 2

Figs. 3 (A) to 3 (E) show the process for fabricating a TFT according to the present Example.

A Corning 7059 glass substrate 31 having a deformation point of 593 °C was heated to a temperature range higher than the deformation point thereof. Thus, the substrate was annealed in the temperature range of from 600 to 660 °C, e.g., at 640 °C, for a duration of from 1 to 4 hours, e.g., for 1 hour, and was gradually cooled at a rate of from 0.1 to 0.5 °C/min, for example, at a rate of



0.2 °C/min. The substrate was taken out from the heating chamber in the temperature range of from 450 to 590 °C, more specifically, at 550 °C.

The substrate 31 thus subjected to the treatment above was cleaned, and a 2,000 Å thick silicon oxide film was deposited as a base film 32 by means of sputtering. An intrinsic (I-type) amorphous silicon film 33 was deposited at a thickness of from 300 to 1,000 Å, for example, at a thickness of 1,000 Å, by effecting plasma CVD. A silicon nitride film from 500 to 2,000 Å in thickness, for instance, at a thickness of 1,000 Å, was deposited continuously. The silicon nitride film thus obtained only was selectively etched to form mask films 34a and 34b (Fig. 3 (A)).

The silicon film was then annealed at 600 °C for a duration of 48 hours under a nitrogen gas atmosphere of 1 atm to crystallize the silicon film. The crystallized silicon film was then allowed to stand in a 100 % by volume water vapor atmosphere under a pressure of 10 atm while maintaining the temperature in the range of from 500 to 600 °C, representatively, at 550 °C, for a duration

of from 3 to 5 hours. Thus, the region of the silicon film not covered by the mask film was completely oxidized to the bottom to form silicon oxide regions 35a to 35c. The silicon region was divided in this manner into regions 36a and 36b (Fig. 3 (B)).

The masks 34a and 34b were removed thereafter, and the surface was globally oxidized again by exposing the resulting structure to an atmosphere containing 100 % water vapor for a duration of from 3 to 5 hours at a temperature of from 500 to 600 °C, representatively, at 550 °C. The surface of the silicon regions 36a and 36b was oxidized in this step to form about 1,000 Å thick oxide films 37a and 37b. The thickness of the silicon region was found to be about 500 Å after this step. The substrate was then left under a nitrous oxide (N<sub>2</sub>O) atmosphere at 600 °C after the oxidation step to provide thermally oxidized films 37a and 37b as the gate dielectric (Fig. 3 (C)).

A silicon film containing from 0.01 to 0.2 % phosphorus was deposited at a thickness of from 3,000 to 8,000 Å, for example, at a thickness of 6,000 Å, by LPCVD. The silicon film was patterned to

form gate electrodes 38n, 38p, and 38c.

Impurities for imparting the region either P- or N-conductive were introduced in a self-aligned manner by means of ion doping process (plasma doping process) into the isolated silicon regions constituting the source/drain and the channel using the gate electrodes as the mask. Phosphine ( $\text{PH}_3$ ) and diborane ( $\text{B}_2\text{H}_6$ ) were used as the doping gas. The dose was from  $1 \times 10^{15}$  to  $8 \times 10^{15}$   $\text{cm}^{-2}$ . Thus, in case phosphine was used, phosphorus was introduced at a dose of, more specifically,  $2 \times 10^{15}$   $\text{cm}^{-2}$ , while applying an accelerating voltage of from 60 to 90 kV, for example, a voltage of 80 kV. In case diborane was used, boron was introduced at a dose of  $5 \times 10^{15}$   $\text{cm}^{-2}$  while applying an accelerating voltage of from 40 to 80 kV, for instance, a voltage of 65 kV. The regions were each selectively doped with the element by covering the other region with a photoresist. Thus were obtained an N-type impurity region 39n and a P-type impurity region 39p to form a region for a P-channel TFT (PTFT) and a region for an N-channel TFT (NTFT).

The regions were then annealed by irradiating a laser beam. A



duration of 30 minutes under a hydrogen gas atmosphere at a pressure of 1 atm (Fig. 3 (E)).

### EXAMPLE 3

Figs. 4 (A) to 4 (E) show the process for fabricating a TFT according to the present Example.

A Corning 7059 glass substrate 42 having a deformation point of 593 °C was heated to a temperature range higher than the deformation point thereof. Thus, the substrate was annealed in the temperature range of from 600 to 660 °C, e.g., at 640 °C, for a duration of from 1 to 4 hours, e.g., for 1 hour, and was gradually cooled at a rate of from 0.1 to 0.5 °C/min, for example, at a rate of 0.2 °C/min. The substrate was taken out from the heating chamber in the temperature range of from 450 to 590 °C, more specifically, at 550 °C. The substrate 42 thus subjected to the treatment above was cleaned, and a 2,000 Å thick silicon oxide film was deposited as a base film 43 by means of plasma CVD using TEOS as the starting material. An intrinsic (I-type) amorphous silicon film

66250 57250 093475 052899

(intrinsic non-single crystal silicon film) 44 was deposited at a thickness of from 100 to 1,000 Å, for example, at a thickness of 300 Å, by effecting plasma CVD. A silicon oxide film 45 having a thickness of 1,000 Å and a silicon nitride film 46 having a thickness of 1,000 Å were deposited continuously. The layers thus obtained were patterned to form a mask.

A thin nickel film from 5 to 20 Å in thickness, for example, 10 Å in thickness, was formed by sputtering. Because this film is extremely thin, it may not be said a film in the strict sense. Thus, the film thickness is an average value. Preferably, the substrate is heated in the range of from 150 to 300 °C during the film deposition. The nickel introduced during this step exerts a catalytic effect on the crystallization of the amorphous silicon layer (Fig. 4 (A)).

The amorphous silicon layer was thermally annealed thereafter at 600 °C for 4 hours in a nitrogen atmosphere under a pressure of 1 atm. The nickel film was found to undergo crystal growth from the selective region on which it was deposited to the region

covered with the mask film along the transverse direction (i.e., the direction in parallel with the substrate). As a result, the amorphous silicon film was crystallized to form a crystalline silicon film 48 (Fig. 4 (B)).

The crystallized silicon film was then allowed to stand in a 100 % by volume water vapor atmosphere under a pressure of 10 atm while maintaining the temperature in the range of from 500 to 600 °C, representatively, at 550 °C, for a duration of 1 hour. Thus, the region of the silicon film not covered by the mask film was completely oxidized to the bottom to form silicon oxide regions 49a and 49b in contact with the side (side plane) of the active layer of the TFT (Fig. 4 (C)).

A silicon oxide film 51 was deposited at a thickness of 1,200 Å by plasma CVD to provide a gate dielectric. Subsequently, an aluminum film containing from 0.01 to 0.2 % of scandium was deposited by sputtering to a thickness of from 6,000 to 8,000 Å, specifically at 6,000 Å, and was patterned to form gate electrodes. The surface of the gate electrodes was covered with an anodic

oxide layer by anodically oxidizing the surface thereof. The anodic oxidation was effected in an ethylene glycol solution containing from 1 to 5 % tartaric acid. The oxide layer thus obtained was 2,000 Å in thickness. Since the oxide layer can be formed to such a thickness capable of forming an offset gate region, the length of the offset gate region can be determined by the anodic oxidation step. Thus were obtained the gate electrode portion 52n, 52p, and 52c inclusive of gate electrode and the peripheral anodic oxide layer.

Impurities for rendering the crystalline silicon region 50 either N-type or P-type conductive were introduced in a self-aligned manner by ion doping using the gate electrode portion as the mask. Phosphine ( $\text{PH}_3$ ) and diborane ( $\text{B}_2\text{H}_6$ ) were used as the doping gas. The dose was from  $1 \times 10^{15}$  to  $8 \times 10^{15} \text{ cm}^{-2}$ . Thus, in case phosphine was used, phosphorus was introduced at a dose of, more specifically,  $2 \times 10^{15} \text{ cm}^{-2}$ , while applying an accelerating voltage of from 60 to 90 kV, for example, a voltage of 80 kV. In case diborane was used, boron was introduced at a dose of  $5 \times 10^{15} \text{ cm}^{-2}$



while applying an accelerating voltage of from 40 to 80 kV, for instance, a voltage of 65 kV. The regions were each selectively doped with the element by covering the other region with a photoresist. Thus were obtained an N-type impurity region 53n and a P-type impurity region 53p to form a region for a P-channel TFT (PTFT) and a region for an N-channel TFT (NTFT).

The regions were then annealed by irradiating a laser beam. A KrF excimer laser operating at a wavelength of 248 nm and at a pulse width of 20 nsec was used in the present invention. However, the type of the laser is not only limited thereto, and any other type of laser can be used as well. The laser beam was irradiated from 2 to 10 shots per site, for example, 2 shots per site, at an energy density of from 200 to 400 mJ/cm<sup>2</sup>, for instance, at 250 mJ/cm<sup>2</sup>. The effect of laser annealing can be further enhanced by heating the substrate in the temperature range of from about 200 to 450 °C. As mentioned in the foregoing, the gate electrode is offset by a length  $y$  corresponding to the thickness of the anodic oxide layer from the impurity region (Fig. 4 (D)).

093475-05280  
068250-ST-22E60

A 6,000 Å thick silicon oxide film 54 was deposited by plasma CVD process thereafter as an interlayer dielectric. Contact holes were formed thereafter to establish electrodes with wiring 55a, 55b, and 55c for the TFT using a metallic material, for example, a multilayered film of titanium nitride and aluminum. A semiconductor circuit comprising the TFTs in a complementary arrangement was obtained by finally annealing the structure at a temperature of 350 °C for a duration of 30 minutes under a hydrogen gas atmosphere at a pressure of 1 atm (Fig. 4 (E)).

#### EXAMPLE 4

Figs. 6 (A) to 6 (E) show the process for fabricating a TFT-type active matrix circuit for use in liquid crystal displays according to the present Example.

A Corning 7059 glass substrate 56 having an insulating surface and a deformation point of 593 °C was heated to a temperature range higher than the deformation point thereof. Thus, the substrate was annealed in the temperature range of from 600

09324715-052899

to 660 °C, e.g., at 640 °C, for a duration of from 1 to 4 hours, e.g., for 1 hour, and was gradually cooled at a rate of from 0.1 to 0.5 °C/min, for example, at a rate of 0.2 °C/min. The substrate was taken out from the heating chamber in the temperature range of from 450 to 590 °C, more specifically, at 550 °C. The substrate 56 thus subjected to the treatment above was cleaned, and a 2,000 Å thick silicon oxide film was deposited as a base film 57 by means of plasma CVD using TEOS as the starting material. An intrinsic (I-type) amorphous silicon film (intrinsic non-single crystal silicon film) 58 was deposited by plasma CVD at a thickness of from 100 to 1,000 Å, for example, at a thickness of 800 Å. A silicon oxide film 59 having a thickness of 1,000 Å and a silicon nitride film 60 having a thickness of 1,000 Å were deposited continuously. The layers thus obtained were patterned to form a mask.

A thin nickel film from 5 to 20 Å in thickness, for example, 10 Å in thickness, was formed by sputtering. Because this film is extremely thin, it may not be said a film in a strict sense. Thus, the film thickness in this case is an average value. Preferably, the

substrate is heated in the range of from 150 to 300 °C during the film deposition. The nickel introduced during this step exerts a catalytic effect on the crystallization of the amorphous silicon layer. Boron ions were introduced thereafter into the silicon film 58 at a dose of from  $2 \times 10^{13}$  to  $5 \times 10^{15}$  cm<sup>-2</sup>, for example, at a dose of  $5 \times 10^{15}$  cm<sup>-2</sup> using the mask film 60 as a mask. The boron ions prevents current leak from occurring due to the formation of an N-type layer on the boundary of the silicon oxide. That is, the boron ions function as the so-called channel stoppers which more clearly isolate the TFTs (Fig. 6 (A)).

The amorphous silicon layer was thermally annealed thereafter at 600 °C for 4 hours in a nitrogen atmosphere under a pressure of 1 atm. The nickel film was found to undergo crystal growth from the selective region on which it was deposited to the region covered with the mask film along the transverse direction (i.e., the direction in parallel with the substrate). After the crystallization, the silicon layer was etched using the mask film 60 as the mask to reduce the thickness thereof to a half of the initial, i.e., from 800

Å to 400 Å (Fig. 6 (B)).

The crystallized silicon film was then allowed to stand in an oxygen atmosphere containing 10 % water vapor under a pressure of 10 atm while maintaining the temperature in the range of from 500 to 600 °C, representatively, at 550 °C, for a duration of 3 hours. Thus, the region of the thin silicon film not covered by the mask film was completely oxidized from a surface thereof through the mask film to form silicon oxide regions 63a and 63b. The pressure of the water vapor was controlled by pyrogenic oxidation. As a result, the silicon film was converted into a silicon oxide layer having a thickness about twice that of the initial silicon layer. In this manner, a silicon oxide region 63 was formed at the same height as those of the region 64 remaining as silicon in the periphery thereof (Fig. 6 (C)).

A silicon oxide film 65 was deposited at a thickness of 1,200 Å by plasma CVD to provide a gate dielectric. Subsequently, an aluminum film containing from 0.01 to 0.2 % of scandium was deposited by sputtering to a thickness of from 6,000 to 8,000 Å,

specifically at 6,000 Å, and was patterned to form a gate electrode. The surface of the aluminum gate electrode was covered with an anodic oxide layer by anodically oxidizing the surface thereof. The anodic oxidation was effected in an ethylene glycol solution containing from 1 to 5 % tartaric acid. The oxide layer thus obtained was 2,000 Å in thickness. Since the oxide layer can be formed to such a thickness capable of forming an offset gate region, the length of the offset gate region can be determined by the anodic oxidation step. Thus was obtained a gate electrode portion 66 inclusive of gate electrode and the peripheral anodic oxide layer. Since the silicon region 64 and the silicon oxide region 63 were formed at approximately the same height, no failures such as disconnection were found to occur on the gate electrode.

Impurities for rendering the crystalline silicon region 64 N-type conductive was introduced in a self-aligned manner by ion doping (plasma doping) using the gate electrode portion as the mask. Phosphine ( $\text{PH}_3$ ) was used as the doping gas. The dose was from  $1 \times 10^{15}$  to  $8 \times 10^{15} \text{ cm}^{-2}$ . Thus, phosphorus was introduced at

09341715-052899  
a dose of, more specifically,  $2 \times 10^{15} \text{ cm}^{-2}$ , while applying an accelerating voltage of from 60 to 90 kV, for example, a voltage of 80 kV. Thus were obtained N-type impurity regions 67a and 67b to form a region for an N-channel TFT (NTFT).

The regions were then annealed by irradiating a laser beam. A KrF excimer laser operating at a wavelength of 248 nm and at a pulse width of 20 nsec was used in the present example. However, the type of the laser is not only limited thereto, and any other type of laser can be used as well. The laser beam was irradiated from 2 to 10 shots per site, for example, 2 shots per site, at an energy density of from 200 to 400 mJ/cm<sup>2</sup>, for instance, at 250 mJ/cm<sup>2</sup>. The effect of laser annealing can be further enhanced by heating the substrate in the temperature range of from about 200 to 450 °C (Fig. 6 (D)).

A 6,000 Å thick silicon oxide film 68 was deposited by plasma CVD process thereafter as an interlayer dielectric. A 800 Å thick ITO film was deposited thereafter by sputtering, and was patterned to provide a pixel electrode 69. Contact holes were formed

thereafter in the interlayer dielectric to establish electrodes with wiring 70a and 70b for the TFT using a metallic material, for example, a multilayered film of titanium nitride and aluminum. A semiconductor circuit (semiconductor device) comprising the TFTs in a complementary arrangement was obtained by finally annealing the structure at a temperature of 350 °C for a duration of 30 minutes under a hydrogen gas atmosphere at a pressure of 1 atm (Fig. 6 (E)).

The product yield of the TFT was thus improved by the present invention. It can be seen that the process according to the present invention can be performed free from the limitations on the base film, and enables use of a film deposition process suitable for mass production. Thus, the present invention is of great use in the industry.

While the invention has been described in detail and with reference to specific embodiments thereof, it will be apparent to one skilled in the art that various changes and modifications can be made therein without departing from the spirit and scope thereof.



WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor device comprising the steps of:

5 forming a semiconductor film comprising silicon over a glass substrate;

crystallizing said semiconductor film; and

oxidizing the crystallized semiconductor film at a pressure higher than 1 atm.

10 2. A method according to claim 1, wherein said pressure is in a range of 1 to 15 atms.

3. A method according to claim 1, wherein said oxidizing is performed in an oxidizing atmosphere.

4. A method according to claim 1, wherein said oxidizing is performed in an oxidizing atmosphere containing water vapor.

15 5. A method according to claim 1, wherein said oxidizing the semiconductor film is performed in a temperature of 500 to 650°C.

6. A method according to claim 1, wherein said semiconductor film has a thickness of 100 to 1,000 Å.

7. A method according to claim 1, wherein at least one region of the semiconductor film is completely oxidized to a bottom surface of the semiconductor film during said oxidizing step.

8. A method according to claim 1, wherein said semiconductor device comprises an active matrix type display device.

9. A method of manufacturing a semiconductor device comprising the steps of:

forming a semiconductor film comprising silicon on an insulating surface;

10 crystallizing said semiconductor film; and

oxidizing the crystallized semiconductor film at a pressure higher than 1 atm.

10. A method according to claim 9, wherein said pressure is in a range of 1 to 15 atms.

11. A method according to claim 9, wherein said oxidizing is performed in an oxidizing atmosphere.

12. A method according to claim 9, wherein said oxidizing is performed in an oxidizing atmosphere containing water vapor.

13. A method according to claim 9, wherein said oxidizing the semiconductor film is performed in a temperature of 500 to 650°C.

14. A method according to claim 9, wherein said semiconductor film has a thickness of 100 to 1,000 Å.

15. A method according to claim 9, wherein at least one region of the semiconductor film is completely oxidized to a bottom surface of the semiconductor film during said oxidizing step.

16. A method according to claim 9, wherein said semiconductor device comprises an active matrix type display device.

17. A method of manufacturing a semiconductor device comprising the steps of:

10           forming a semiconductor film comprising silicon over an alkali-free glass substrate;  
              crystallizing said semiconductor film; and  
              oxidizing the crystallized semiconductor film at a pressure higher than 1 atm.

15           18. A method according to claim 17, wherein said pressure is in a range of 1 to 15 atms.

19. A method according to claim 17, wherein said oxidizing is performed in an oxidizing atmosphere.

20           20. A method according to claim 17, wherein said oxidizing is performed in an oxidizing atmosphere containing water vapor.

21. A method according to claim 17, wherein said oxidizing the semiconductor film is performed in a temperature of 500 to 650°C.

22. A method according to claim 17, wherein said semiconductor film has a thickness of 100 to 1,000 Å.

5           23. A method according to claim 17, wherein at least one region of the semiconductor film is completely oxidized to a bottom surface of the semiconductor film during said oxidizing step.

24. A method according to claim 17, wherein said semiconductor device comprises an active matrix type display device.

10           25. A method of manufacturing a semiconductor device comprising the steps of:

forming a semiconductor film comprising silicon over a glass substrate;

crystallizing said semiconductor film;

15           forming a gate insulating film adjacent to said crystallized semiconductor film; and

forming a gate electrode adjacent to said gate insulating film, wherein said method further comprises a step of oxidizing the crystallized semiconductor film at a pressure higher than 1 atm.

20           26. A method according to claim 25, wherein said pressure is in a range of 1 to 15 atms.

27. A method according to claim 25, wherein said semiconductor device comprising at least one top gate type thin film transistor.

28. A method according to claim 25, wherein said oxidizing is performed in an oxidizing atmosphere containing water vapor.

5 29. A method according to claim 25, wherein said oxidizing the semiconductor film is performed in a temperature of 500 to 650°C.

30. A method according to claim 25, wherein said semiconductor film has a thickness of 100 to 1,000 Å.

10 31. A method according to claim 25, wherein at least one region of the semiconductor film is completely oxidized to a bottom surface of the semiconductor film during said oxidizing step.

32. A method according to claim 25, wherein said semiconductor device comprises an active matrix type display device.

15 33. A method of manufacturing a semiconductor device comprising the steps of:

forming a semiconductor film comprising silicon on an insulating surface;

crystallizing said semiconductor film;

20 forming a gate insulating film adjacent to said crystallized semiconductor film; and

forming a gate electrode adjacent to said gate insulating film,

wherein said method further comprises a step of oxidizing the crystallized semiconductor film at a pressure higher than 1 atm.

34. A method according to claim 33, wherein said pressure is in a range of 1 to 15 atms.

5 35. A method according to claim 33, wherein said semiconductor device comprising at least one top gate type thin film transistor.

36. A method according to claim 33, wherein said oxidizing is performed in an oxidizing atmosphere containing water vapor.

10 37. A method according to claim 33, wherein said oxidizing the semiconductor film is performed in a temperature of 500 to 650°C.

38. A method according to claim 33, wherein said semiconductor film has a thickness of 100 to 1,000 Å.

15 39. A method according to claim 33, wherein at least one region of the semiconductor film is completely oxidized to a bottom surface of the semiconductor film during said oxidizing step.

40. A method according to claim 33, wherein said semiconductor device comprises an active matrix type display device.

41. A method of manufacturing a semiconductor device comprising the steps of:

forming a semiconductor film comprising silicon over an alkali-free glass substrate;

crystallizing said semiconductor film;

5 forming a gate insulating film adjacent to said crystallized semiconductor film; and

forming a gate electrode adjacent to said gate insulating film, wherein said method further comprises a step of oxidizing the crystallized semiconductor film at a pressure higher than 1 atm.

10 42. A method according to claim 41, wherein said pressure is in a range of 1 to 15 atms.

43. A method according to claim 41, wherein said semiconductor device comprising at least one top gate type thin film transistor.

44. A method according to claim 41, wherein said oxidizing is performed in an oxidizing atmosphere containing water vapor.

15 45. A method according to claim 41, wherein said oxidizing the semiconductor film is performed in a temperature of 500 to 650°C.

46. A method according to claim 41, wherein said semiconductor film has a thickness of 100 to 1,000 Å.

20 47. A method according to claim 41, wherein at least one region of the semiconductor film is completely oxidized to a bottom surface of the semiconductor film during said oxidizing step.

48. A method according to claim 41, wherein said semiconductor device comprises an active matrix type display device.

49. A method of manufacturing a semiconductor device comprising the steps of:

5 forming a semiconductor film comprising silicon over a glass substrate;

crystallizing said semiconductor film; and

heating the crystallized semiconductor film in an oxidizing atmosphere at a pressure higher than 1 atm.

10 50. A method according to claim 49, wherein said pressure is in a range of 1 to 15 atms.

51. A method according to claim 49, wherein said oxidizing atmosphere contains water vapor.

15 52. A method according to claim 49, wherein said heating the semiconductor film is performed in a temperature of 500 to 650°C.

53. A method according to claim 49, wherein said semiconductor film has a thickness of 100 to 1,000 Å.

20 54. A method according to claim 49, wherein at least one region of the semiconductor film is completely oxidized to a bottom surface of the semiconductor film during said heating step.



55. A method according to claim 49, wherein said semiconductor device comprises an active matrix type display device.

56. A method of manufacturing a semiconductor device comprising the steps of:

5 forming a semiconductor film comprising silicon on an insulating surface;

crystallizing said semiconductor film; and

heating the crystallized semiconductor film in an oxidizing atmosphere at a pressure higher than 1 atm.

10 57. A method according to claim 56, wherein said pressure is in a range of 1 to 15 atms.

58. A method according to claim 56, wherein said oxidizing atmosphere contains water vapor.

15 59. A method according to claim 56, wherein said heating the semiconductor film is performed in a temperature of 500 to 650°C.

60. A method according to claim 56, wherein said semiconductor film has a thickness of 100 to 1,000 Å.

20 61. A method according to claim 56, wherein at least one region of the semiconductor film is completely oxidized to a bottom surface of the semiconductor film during said heating step.

62. A method according to claim 56, wherein said semiconductor device comprises an active matrix type display device.

63. A method of manufacturing a semiconductor device comprising the steps of:

5 forming a semiconductor film comprising silicon over an alkali-free glass substrate;

crystallizing said semiconductor film; and

heating the crystallized semiconductor film in an oxidizing atmosphere at a pressure higher than 1 atm.

10 64. A method according to claim 63, wherein said pressure is in a range of 1 to 15 atms.

65. A method according to claim 63, wherein said oxidizing atmosphere contains water vapor.

15 66. A method according to claim 63, wherein said heating the semiconductor film is performed in a temperature of 500 to 650°C.

67. A method according to claim 63, wherein said semiconductor film has a thickness of 100 to 1,000 Å.

20 68. A method according to claim 63, wherein at least one region of the semiconductor film is completely oxidized to a bottom surface of the semiconductor film during said heating step.

69. A method according to claim 63, wherein said semiconductor device comprises an active matrix type display device.

70. A method of manufacturing a semiconductor device comprising the steps of:

5                   forming a semiconductor film comprising silicon over a glass substrate;

                  crystallizing said semiconductor film;

                  forming a gate insulating film adjacent to said crystallized semiconductor film; and

10                  forming a gate electrode adjacent to said gate insulating film,  
                  wherein said method further comprises a step of heating the crystallized semiconductor film in an oxidizing atmosphere at a pressure higher than 1 atm.

15                  71. A method according to claim 70, wherein said pressure is in a range of 1 to 15 atms.

72. A method according to claim 70, wherein said semiconductor device comprising at least one top gate type thin film transistor.

73. A method according to claim 70, wherein said oxidizing atmosphere contains water vapor.

20                  74. A method according to claim 70, wherein said heating the semiconductor film is performed in a temperature of 500 to 650°C.

75. A method according to claim 70, wherein said semiconductor film has a thickness of 100 to 1,000 Å.

76. A method according to claim 70, wherein at least one region of the semiconductor film is completely oxidized to a bottom surface of the semiconductor film during said oxidizing step.

77. A method according to claim 70, wherein said semiconductor device comprises an active matrix type display device.

78. A method of manufacturing a semiconductor device comprising the steps of:

10 forming a semiconductor film comprising silicon on an insulating surface;

crystallizing said semiconductor film;

forming a gate insulating film adjacent to said crystallized semiconductor film; and

15 forming a gate electrode adjacent to said gate insulating film, wherein said method further comprises a step of heating the crystallized semiconductor film in an oxidizing atmosphere at a pressure higher than 1 atm.

79. A method according to claim 78, wherein said pressure is in a range of 1 to 15 atms.

80. A method according to claim 78, wherein said semiconductor device comprising at least one top gate type thin film transistor.

81. A method according to claim 78, wherein said oxidizing atmosphere contains water vapor.

82. A method according to claim 78, wherein said heating the semiconductor film is performed in a temperature of 500 to 650°C.

5 83. A method according to claim 78, wherein said semiconductor film has a thickness of 100 to 1,000 Å.

84. A method according to claim 78, wherein at least one region of the semiconductor film is completely oxidized to a bottom surface of the semiconductor film during said oxidizing step.

10 85. A method according to claim 78, wherein said semiconductor device comprises an active matrix type display device.

86. A method of manufacturing a semiconductor device comprising the steps of:

15 forming a semiconductor film comprising silicon over an alkali-free glass substrate;

crystallizing said semiconductor film;

forming a gate insulating film adjacent to said crystallized semiconductor film; and

20 forming a gate electrode adjacent to said gate insulating film, wherein said method further comprises a step of heating the crystallized semiconductor film in an oxidizing atmosphere at a pressure higher than 1 atm.

87. A method according to claim 86, wherein said pressure is in a range of 1 to 15 atms.

88. A method according to claim 86, wherein said semiconductor device comprising at least one top gate type thin film transistor.

5 89. A method according to claim 86, wherein said oxidizing atmosphere contains water vapor.

90. A method according to claim 86, wherein said heating the semiconductor film is performed in a temperature of 500 to 650°C.

10 91. A method according to claim 86, wherein said semiconductor film has a thickness of 100 to 1,000 Å.

92. A method according to claim 86, wherein at least one region of the semiconductor film is completely oxidized to a bottom surface of the semiconductor film during said oxidizing step.

15 93. A method according to claim 86, wherein said semiconductor device comprises an active matrix type display device.

# ABSTRACT

A semiconductor device comprising at least two thin film transistors on a substrate having an insulating surface thereon, provided that the thin film transistors are isolated by oxidizing the outer periphery of the active layer of each of the thin film transistors to the bottom to provide an oxide insulating film.

053474-053499

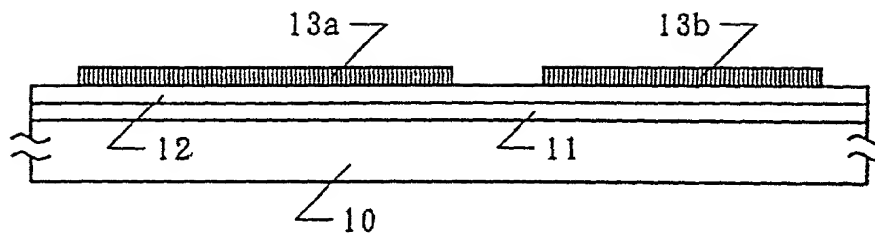


Fig. 1(A)

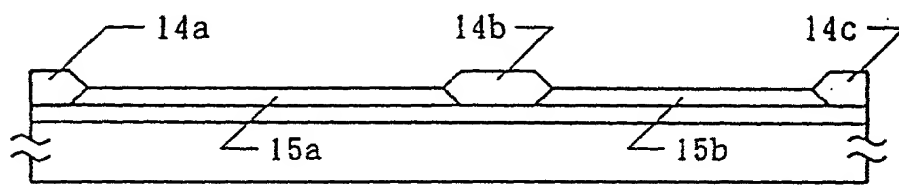


Fig. 1(B)

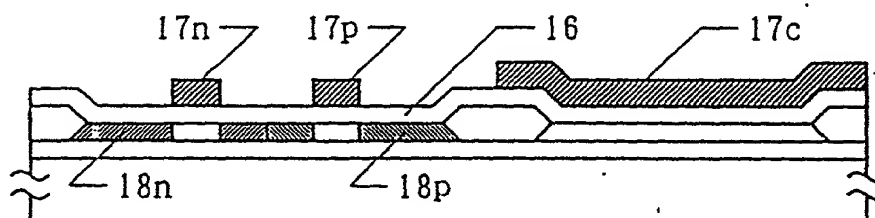


Fig. 1(C)

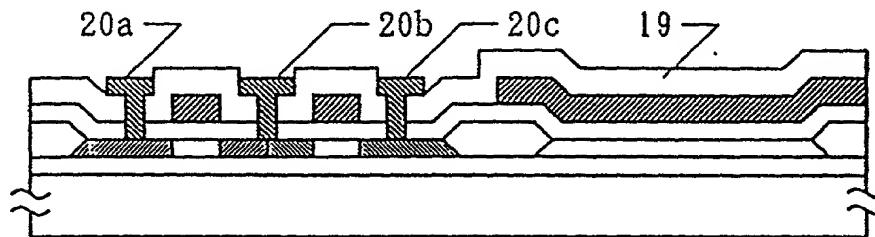


Fig. 1(D)

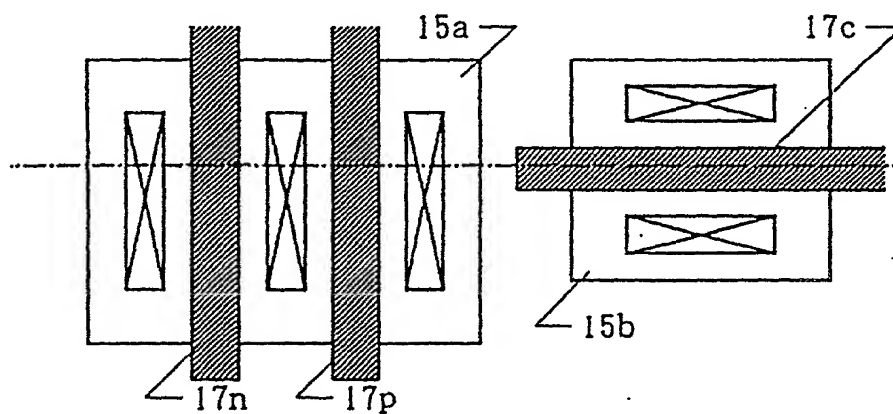


Fig. 1(E)



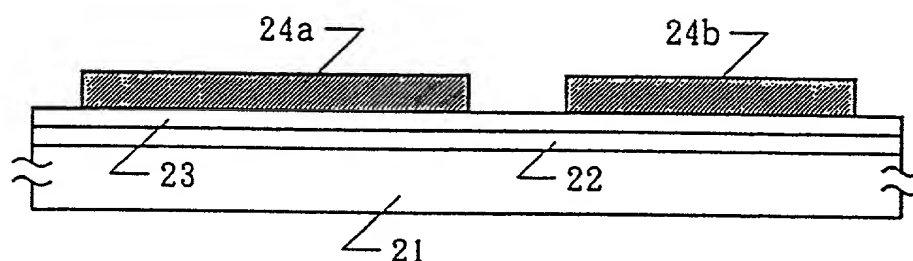


Fig. 2(A)

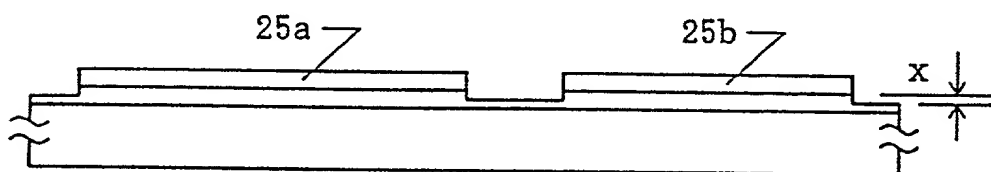


Fig. 2(B)

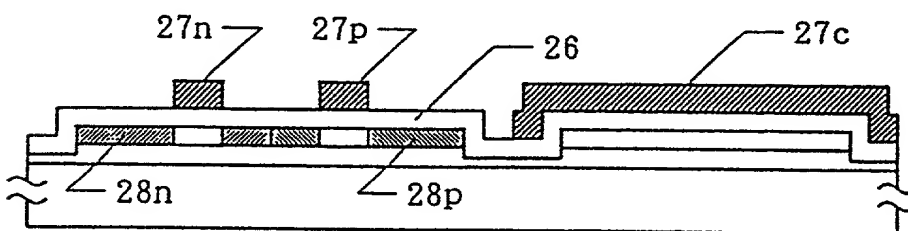


Fig. 2(c)

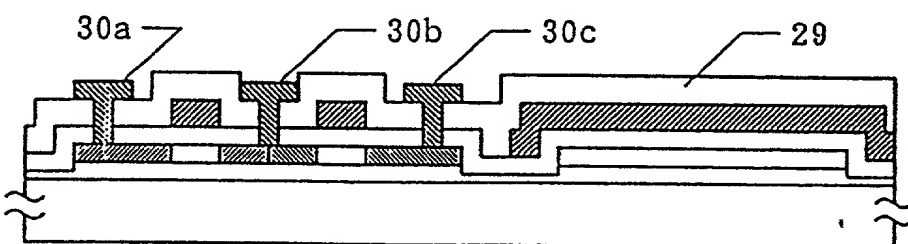


Fig. 2(d)

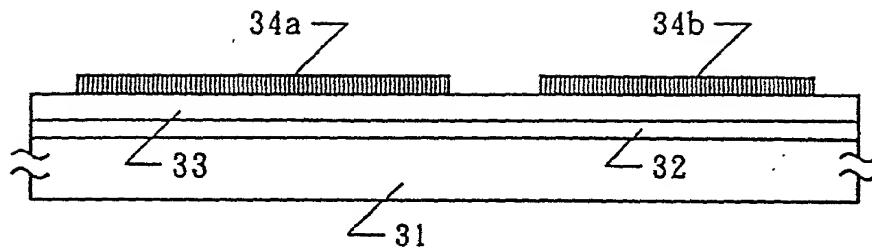


Fig. 3(A)

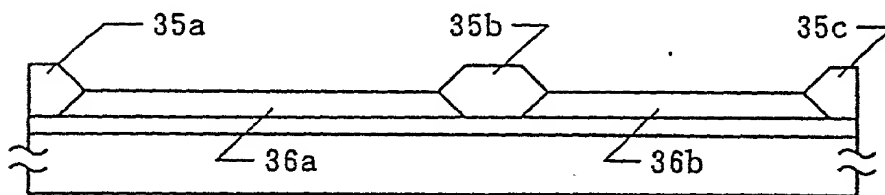


Fig. 3(B)

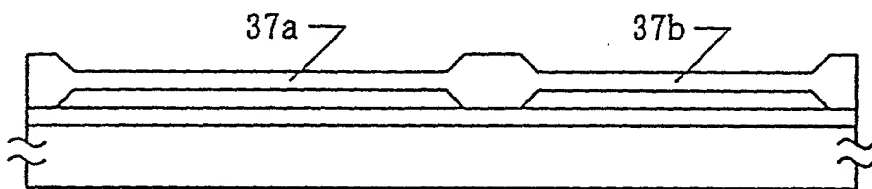


Fig. 3(C)

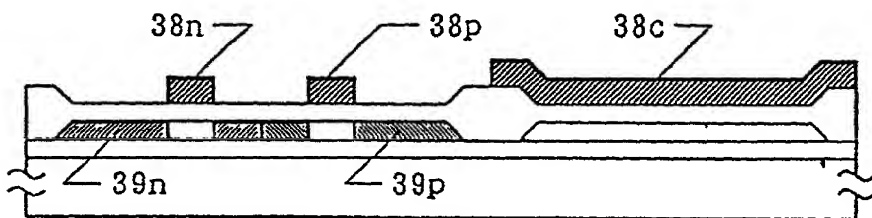


Fig. 3(D)

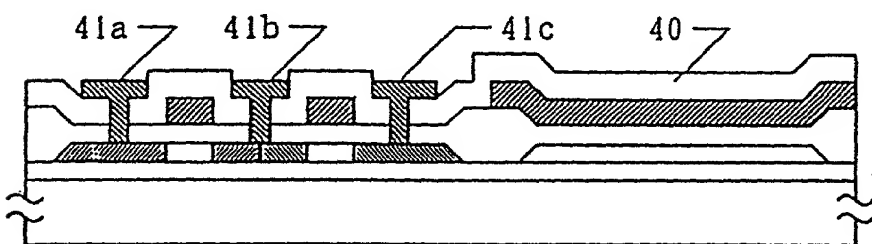


Fig. 3(E)

668260 STZT2660

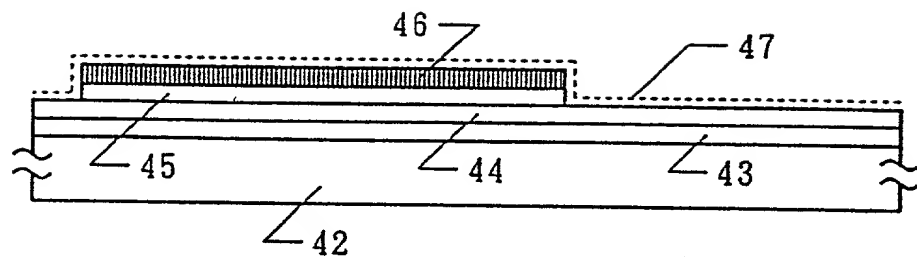


Fig. 4(A)

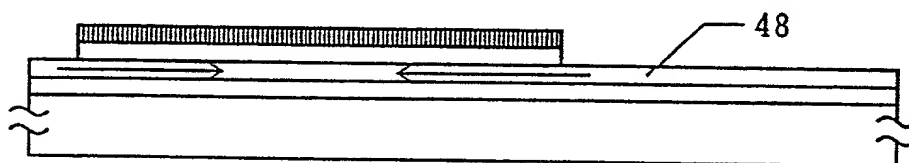


Fig. 4(B)

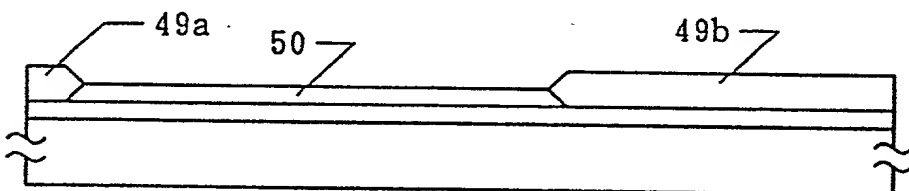


Fig. 4(C)

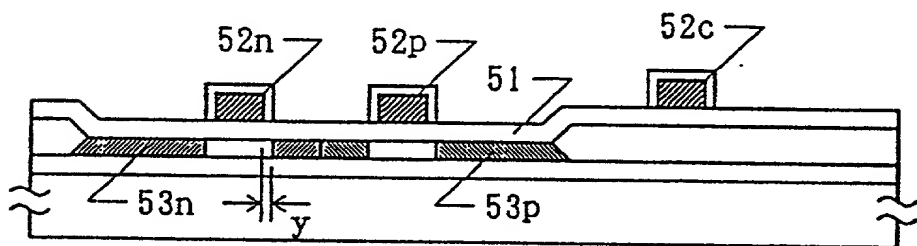


Fig. 4(D)

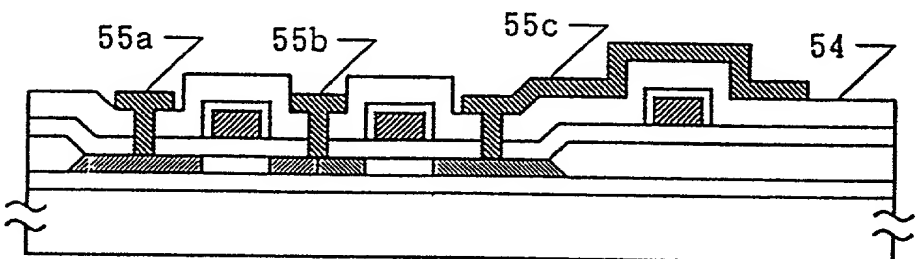
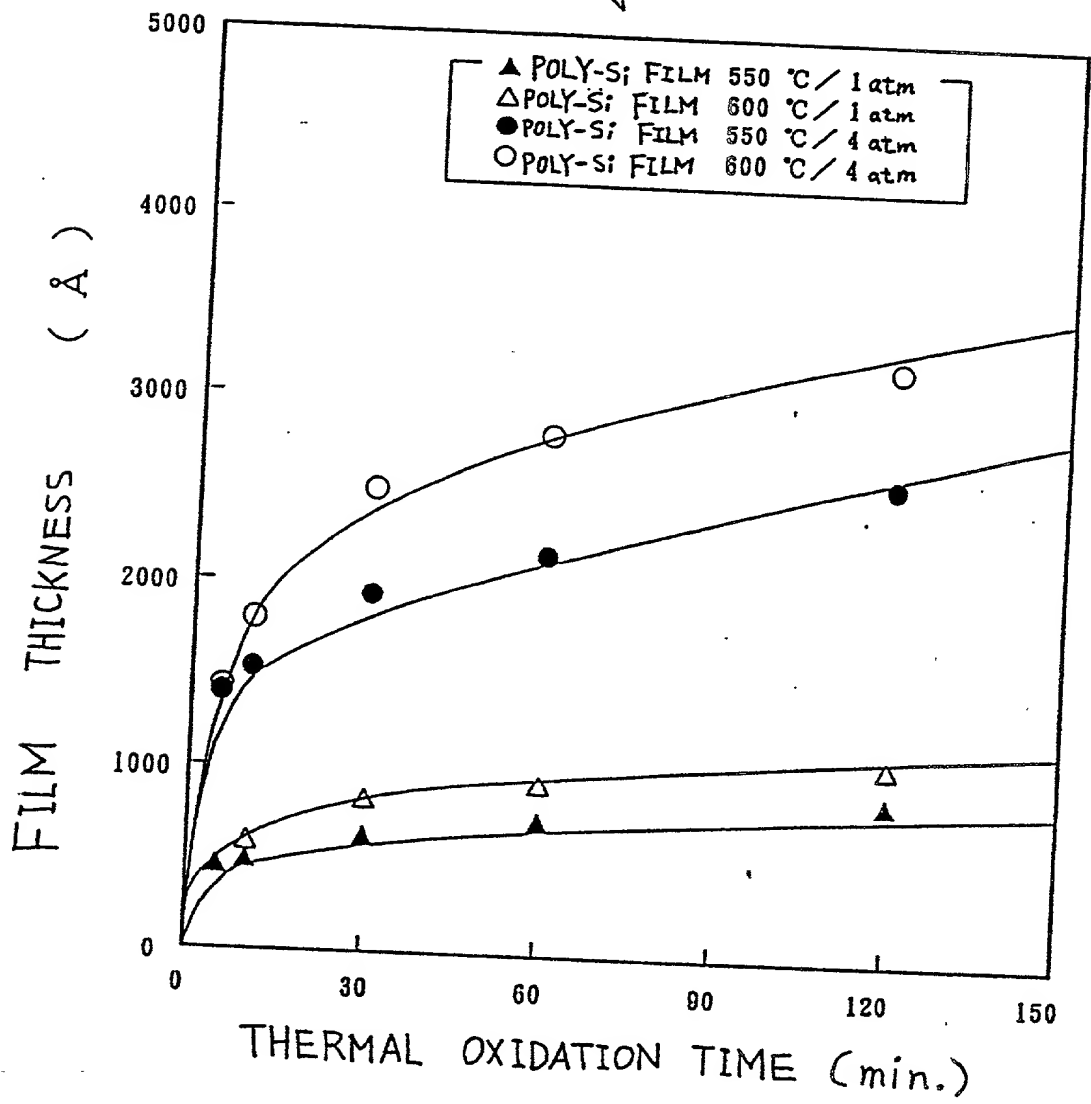


Fig. 4(E)

Fig. 5



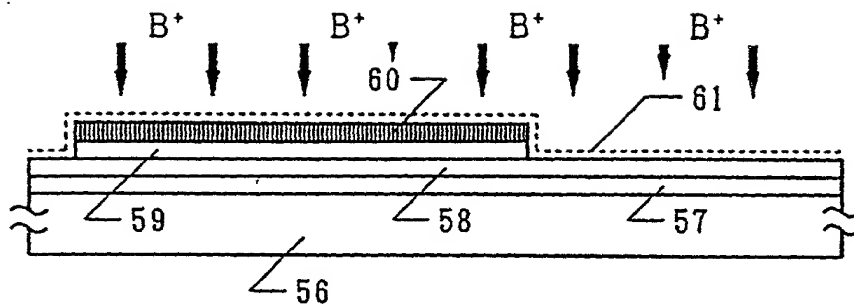


Fig. 6(A)

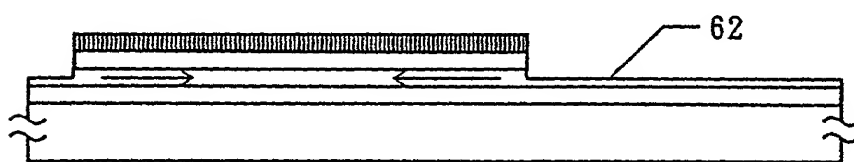


Fig. 6(B)

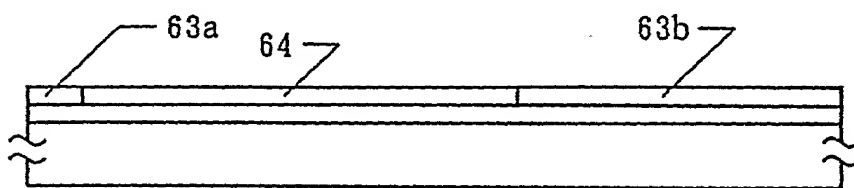


Fig. 6(c)

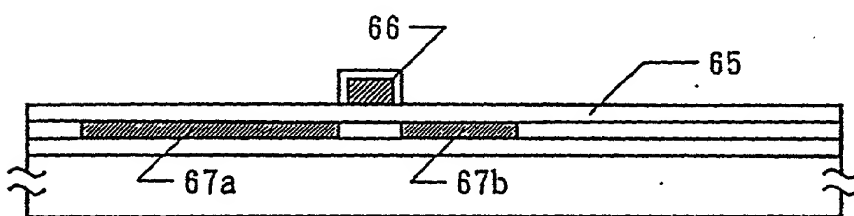


Fig. 6(D)

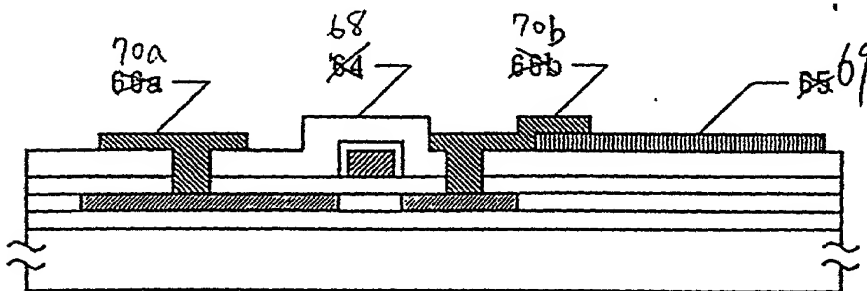


Fig. 6(E)

093215-05259

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re DIVISIONAL Application of )  
Yasuhiko TAKEMURA et al. )  
Based On Serial No. 08/853,187 ) Art Unit: 2822  
Which Was Filed: April 29, 1997 ) Examiner: M. Wilczewski  
For: SEMICONDUCTOR DEVICE AND )  
PROCESS FOR FABRICATING )  
THE SAME ) Date: May 27, 1999

NOTICE OF CHANGE OF ADDRESS

Honorable Assistant Commissioner for Patents  
Washington, D.C. 20231

Sir:

Effective immediately, please note that the address of the attorney(s) of record in the above-referenced application has been changed. Please direct all future correspondence to:

SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, P.C.  
8180 Greensboro Drive, Suite 800  
McLean, Virginia 22102

Telephone (703) 790-9110

Respectfully submitted,



Eric J. Robinson  
Registration No. 38,285

Sixbey, Friedman, Leedom & Ferguson, P.C.  
8180 Greensboro Drive, Suite 800  
McLean, Virginia 22102  
(703) 790-9110

094445-052590

# DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

ATTORNEY DOCKET NO.

PLEASE NOTE:  
YOU MUST  
COMPLETE THIS  
FOLLOWING:

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are named below) of the invention entitled: \* SEMICONDUCTOR DEVICE AND PROCESS FOR FABRICATING THE SAME

\_\_\_\_\_, the specification of which is attached hereto unless the following box is checked:

☐ The specification was filed on \_\_\_\_\_  
and was assigned Serial No. \_\_\_\_\_  
and was amended on \_\_\_\_\_  
(if known)  
(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof, or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application, and that no application for patent or inventor's certificate on this invention has been filed in any country foreign to the United States of America prior to this application by me or my legal representatives or assigns, except as follows:

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and checked at right:

Prior Foreign Application(s)			Priority Claimed	
5-227893 (Number)	JAPAN (Country)	August 20, 1993 (Month/Day/Year Filed)	<input checked="" type="checkbox"/> Yes	<input type="checkbox"/> No
_____ (Number)	_____ (Country)	_____ (Month/Day/Year Filed)	<input type="checkbox"/> Yes	<input type="checkbox"/> No
_____ (Number)	_____ (Country)	_____ (Month/Day/Year Filed)	<input type="checkbox"/> Yes	<input type="checkbox"/> No
_____ (Number)	_____ (Country)	_____ (Month/Day/Year Filed)	<input type="checkbox"/> Yes	<input type="checkbox"/> No
_____ (Number)	_____ (Country)	_____ (Month/Day/Year Filed)	<input type="checkbox"/> Yes	<input type="checkbox"/> No

All Foreign Applications, if any, for any Patent or Inventor's Certificate Filed More Than 12 Months Prior To The Filing Date of This Application:

Country	Application No.	Date of Filing (Month/Day/Year)
_____	_____	_____

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status—patented, pending, abandoned)
_____	_____	_____

\*NOTE: Must be completed.

I hereby appoint the following attorneys to prosecute this application and/or an international application and to transact all business in the Patent and Trademark Office connected therewith:

Daniel W. Sixbey (Reg. No. 20,932)  
 Stuart J. Friedman (Reg. No. 24,312)  
 Charles M. Leedom, Jr. (Reg. No. 26,477)

Gerald J. Ferguson, Jr. (Reg. No. 23,016)  
 David S. Safran (Reg. No. 27,997)  
 Thomas W. Cole (Reg. No. 28,290)

Send Correspondence to:

SIXBEY, FRIEDMAN, LEEDOM & FERGUSON, P.C.  
 2010 Corporate Ridge, Suite 600  
 McLean, Virginia 22102  
 Telephone: (703) 790-9110

PLEASE NOTE:  
 YOU MUST  
 COMPLETE THE  
 FOLLOWING

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

The undersigned hereby authorize any U. S. attorney or agent named herein to accept and follow instructions from \_\_\_\_\_ as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the U. S. attorney or agent and the undersigned. In the event of a change in the persons from whom instructions may be taken, the U.S. attorneys or agents named herein will be so notified by the undersigned.

Insert Full Name of  
 First or Sole Inventor  
 and Date This  
 Document Is Signed

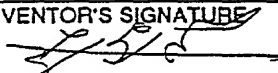

Insert Residence  
 Insert Citizenship

Insert Post Office  
 Address

Second Inventor:  
 see above

Third Inventor:  
 see above

Fourth Inventor:  
 see above

FULL NAME OF SOLE OR FIRST INVENTOR Yasuhiko TAKEMURA	INVENTOR'S SIGNATURE 	DATE 7/30/1994
RESIDENCE (City, State & Country) Kanagawa, Japan		CITIZENSHIP Japanese
POST OFFICE ADDRESS (Complete Street Address including City, State & Country) Flat Atsugi 208, 931-1, Hase, Atsugi-shi, Kanagawa-ken 243 Japan		
FULL NAME OF SECOND JOINT INVENTOR, IF ANY Hiroki ADACHI	INVENTOR'S SIGNATURE 	DATE 7/30/1994
RESIDENCE (City, State & Country) Kanagawa, Japan		CITIZENSHIP Japanese
POST OFFICE ADDRESS (Complete Street Address including City, State & Country) Flat SEL-B 206, 304-1, Hase, Atsugi-shi, Kanagawa-ken 243 Japan		
FULL NAME OF THIRD JOINT INVENTOR, IF ANY	INVENTOR'S SIGNATURE	DATE
RESIDENCE (City, State & Country)		CITIZENSHIP
POST OFFICE ADDRESS (Complete Street Address including City, State & Country)		
FULL NAME OF FOURTH JOINT INVENTOR, IF ANY	INVENTOR'S SIGNATURE	DATE
RESIDENCE (City, State & Country)		CITIZENSHIP
POST OFFICE ADDRESS (Complete Street Address including City, State & Country)		